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FIG. 1

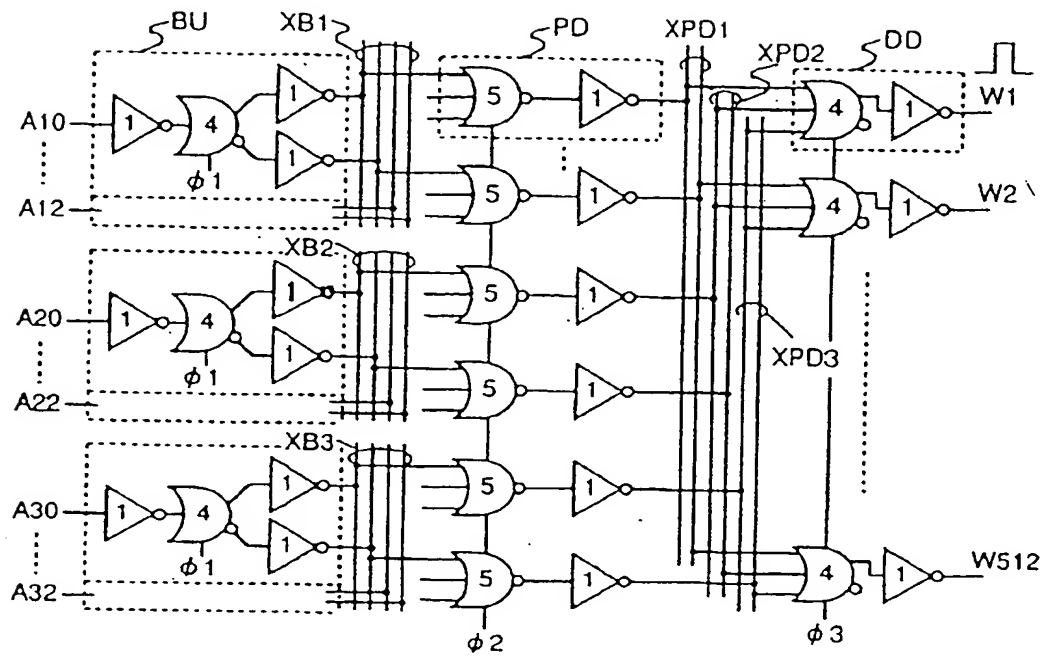


FIG. 2

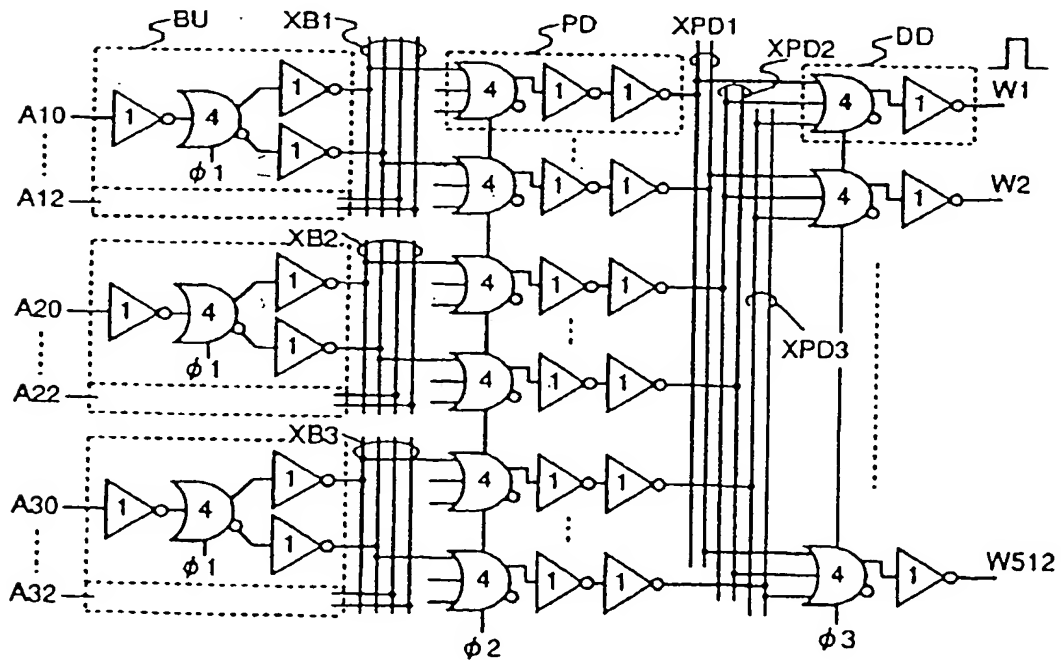


FIG. 3

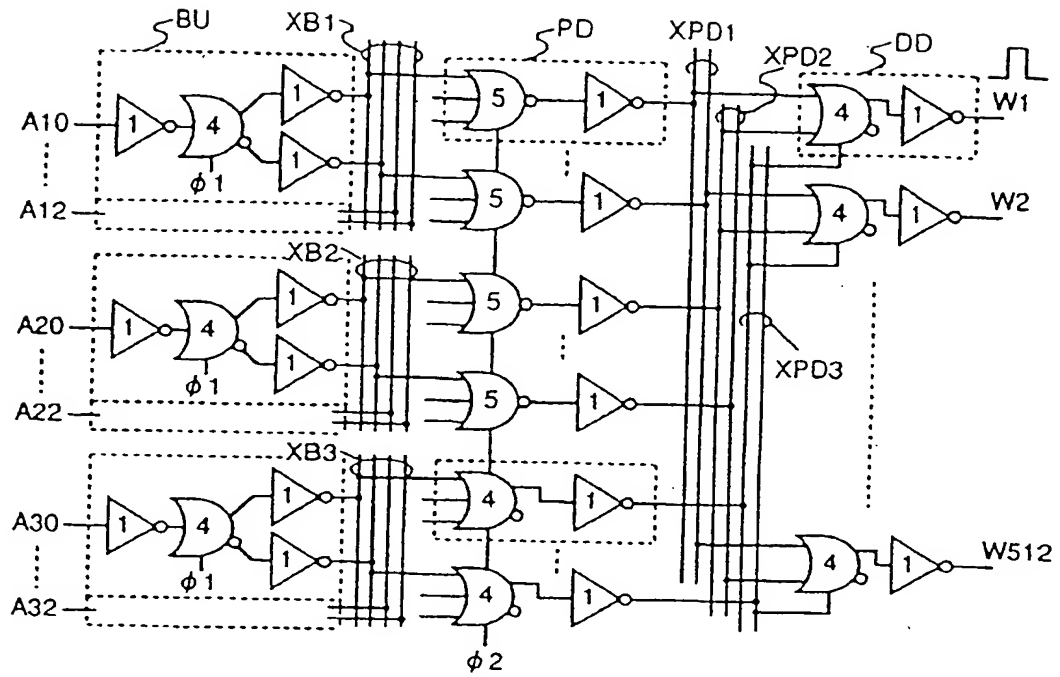


FIG. 4

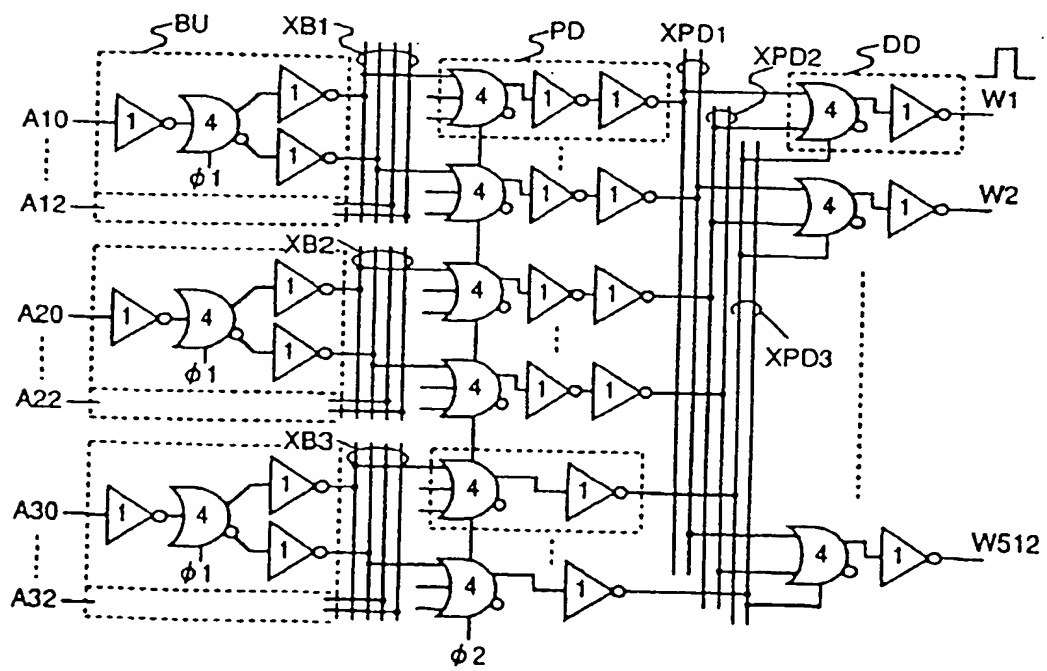


FIG. 5

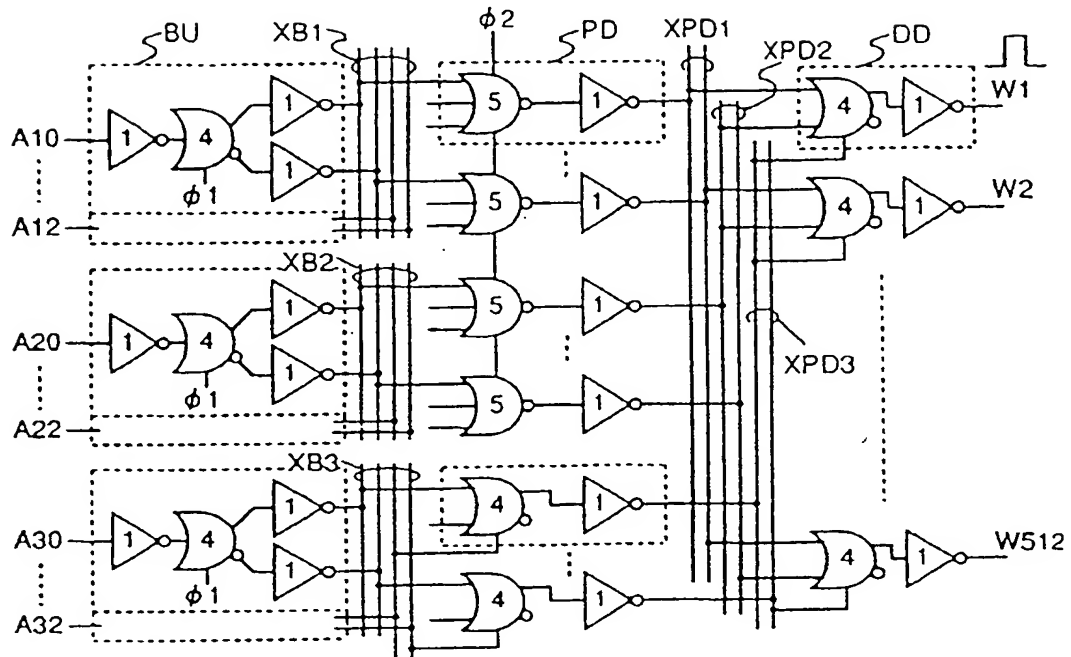


FIG. 6

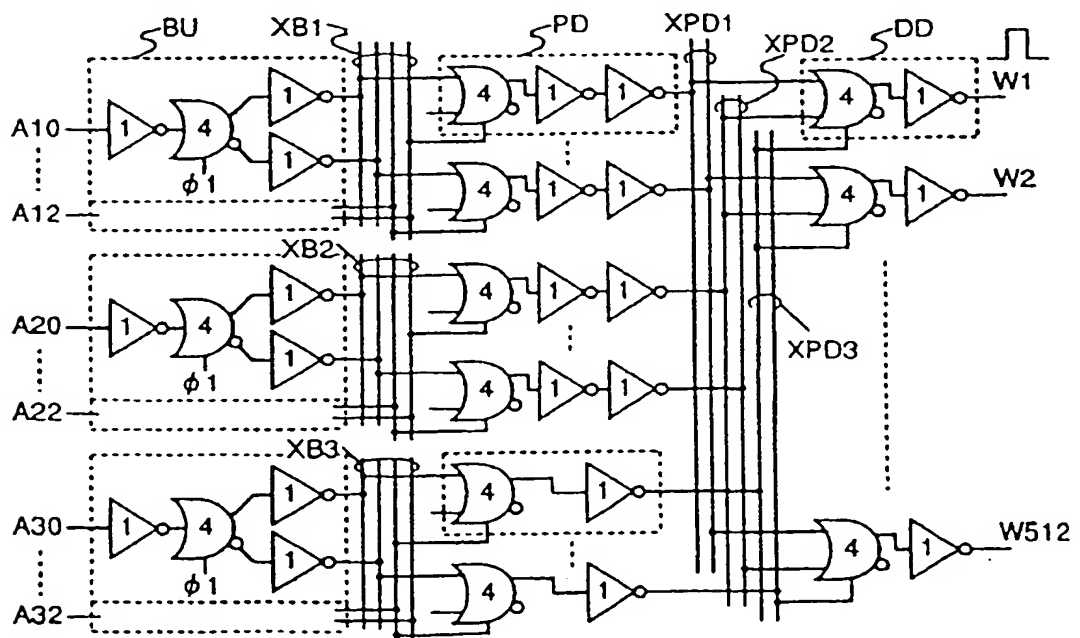


FIG. 7

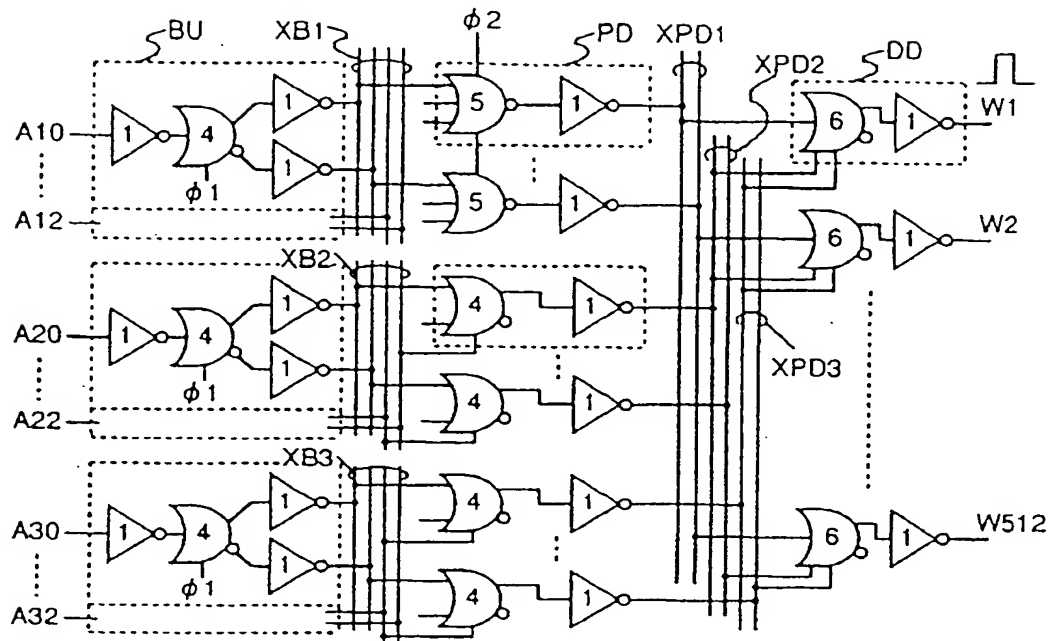


FIG. 8

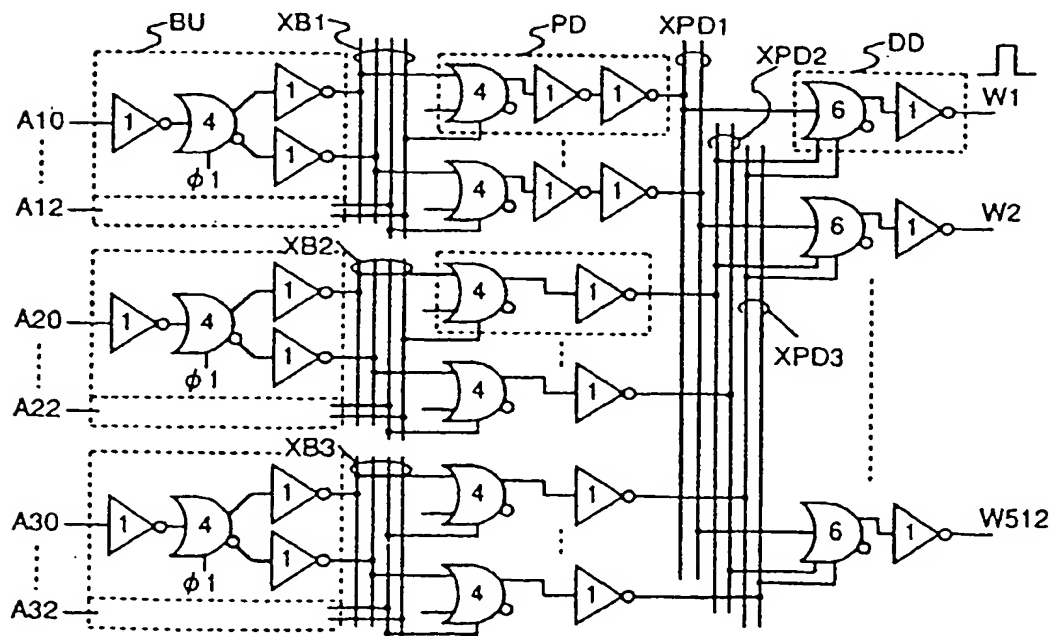


FIG. 9

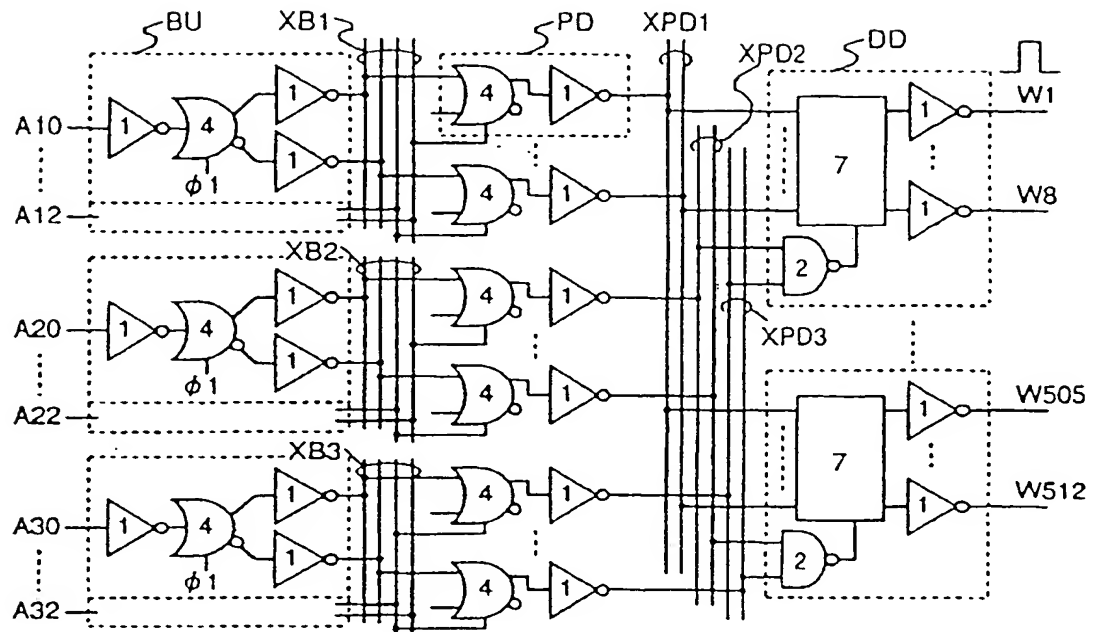


FIG. 10

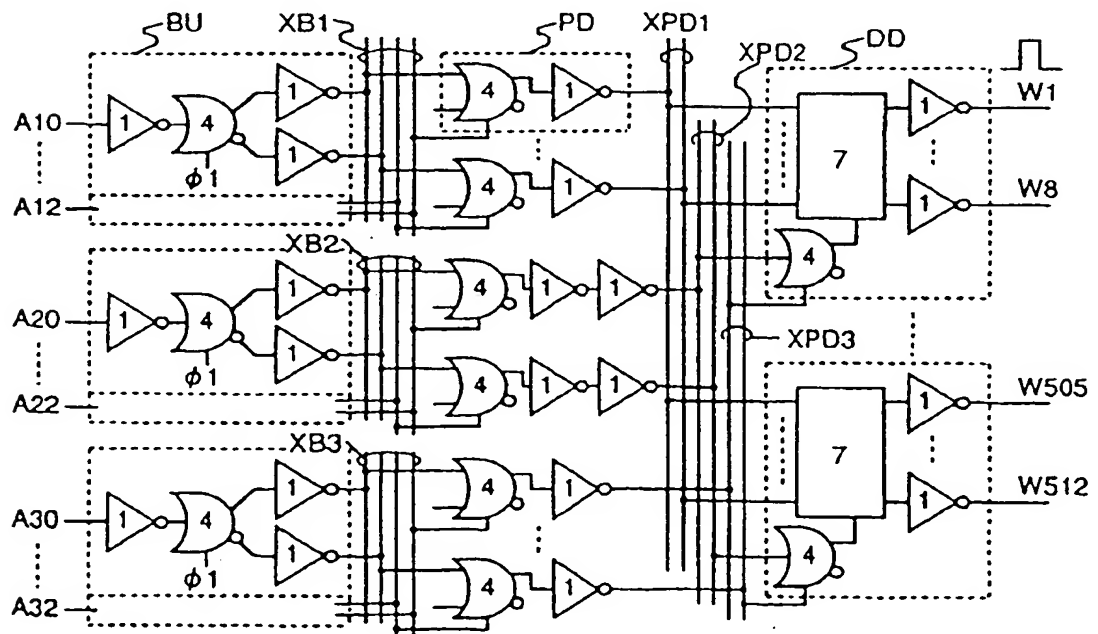


FIG. 11

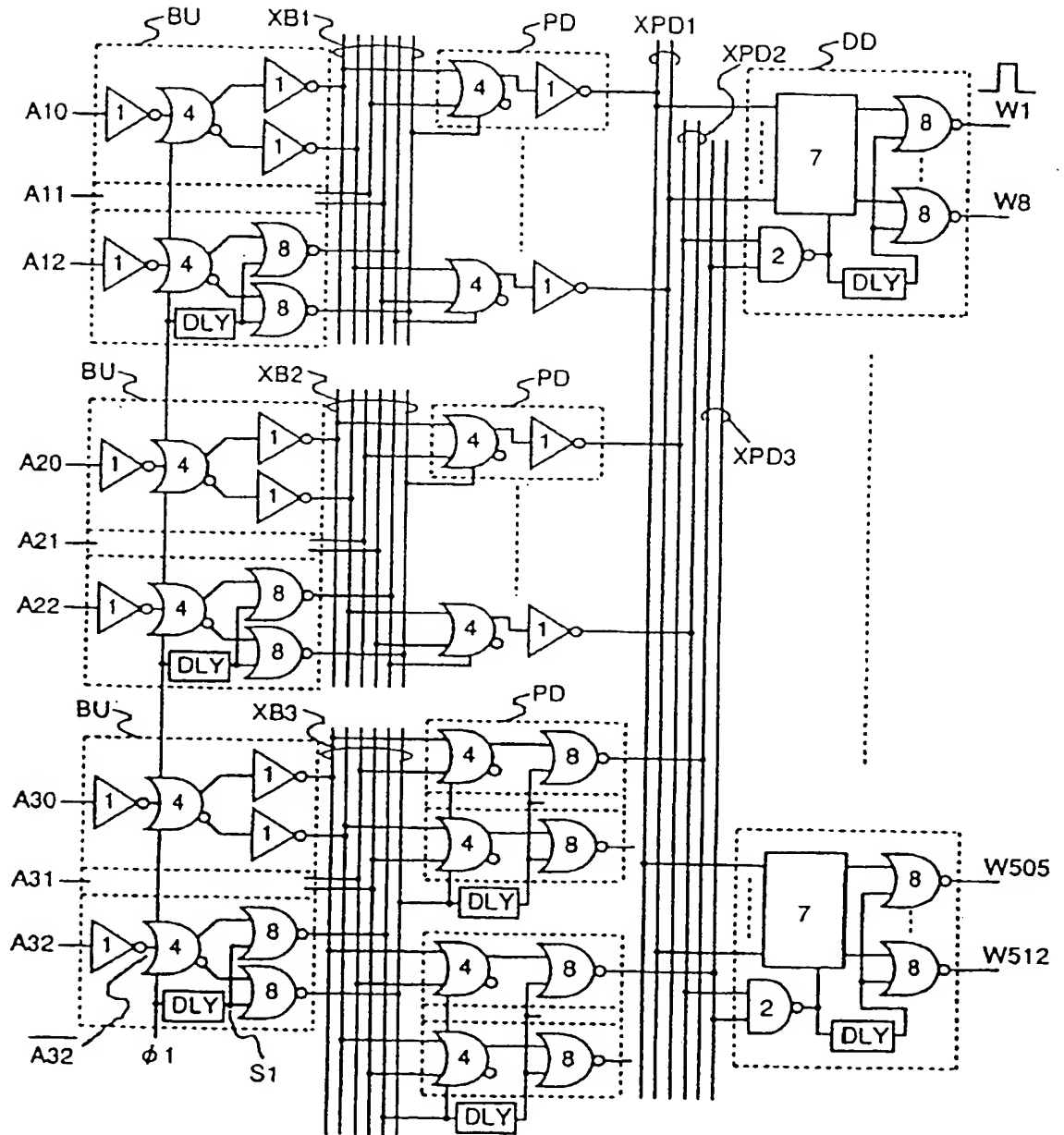


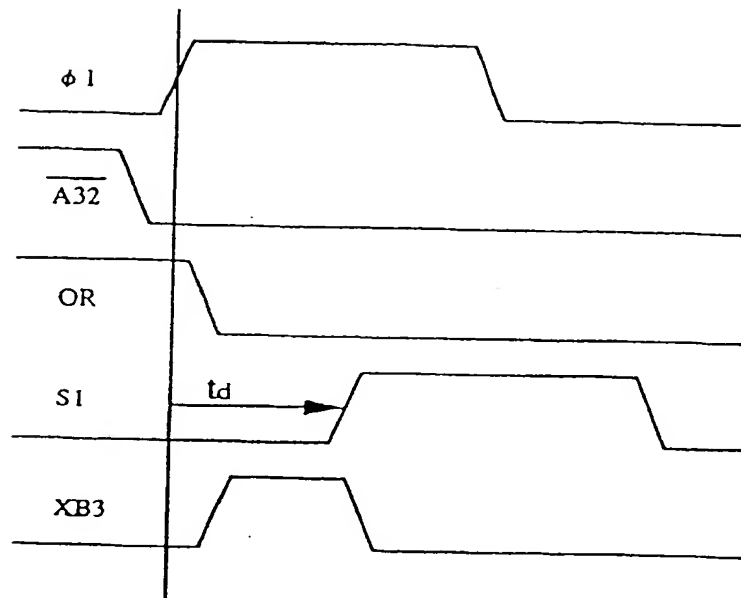
FIG. 12

FIG. 13(a)

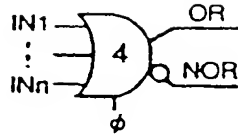
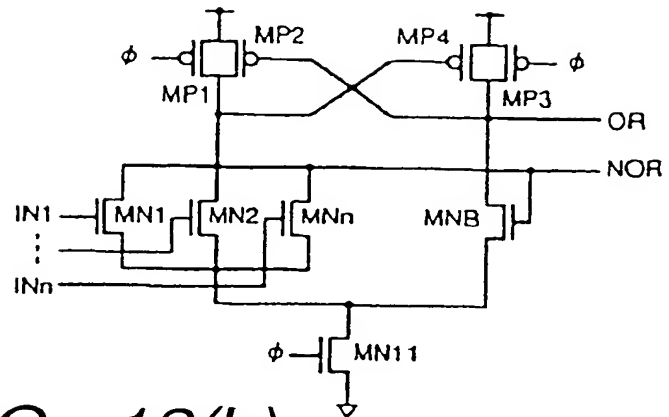


FIG. 13(b)

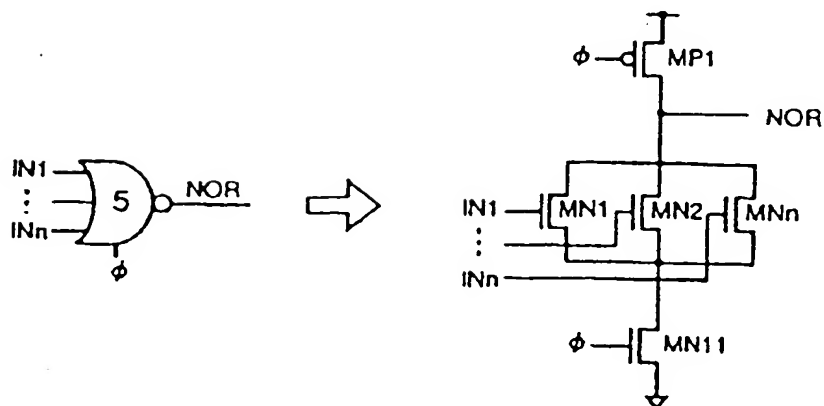
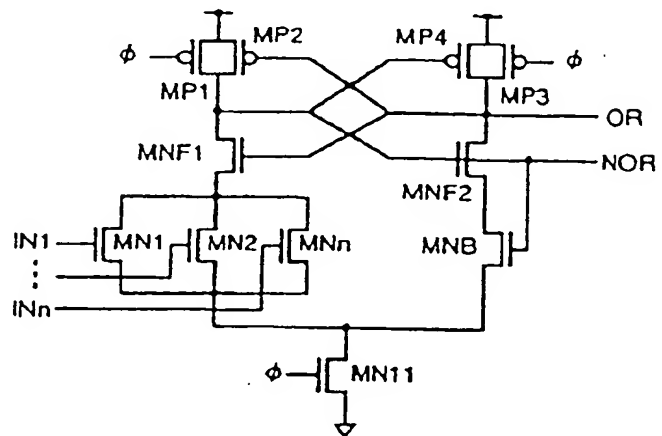
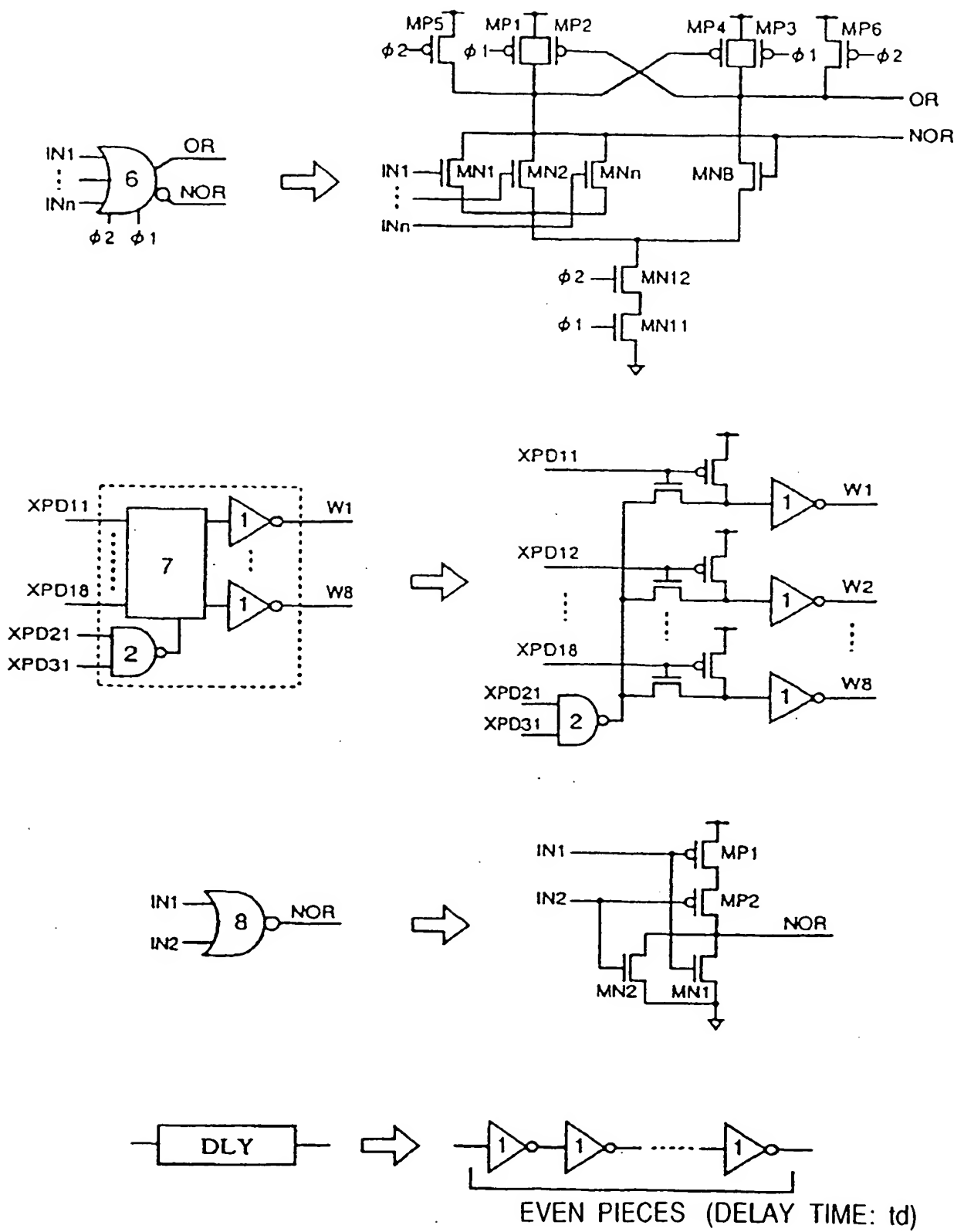


FIG. 14



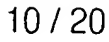


FIG. 16 PRIOR ART

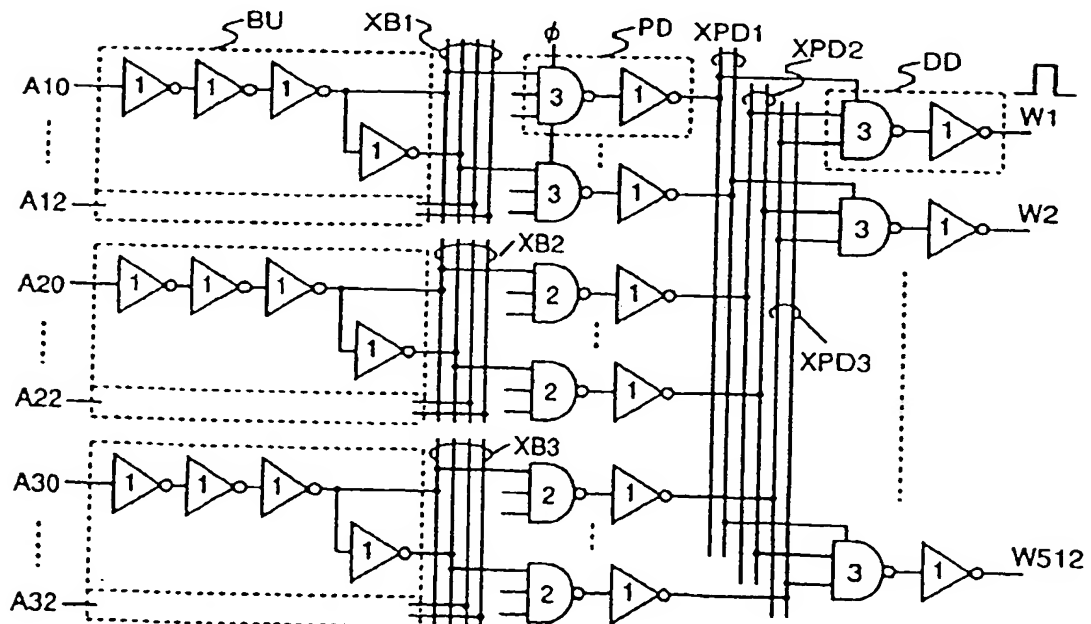


FIG. 17 PRIOR ART

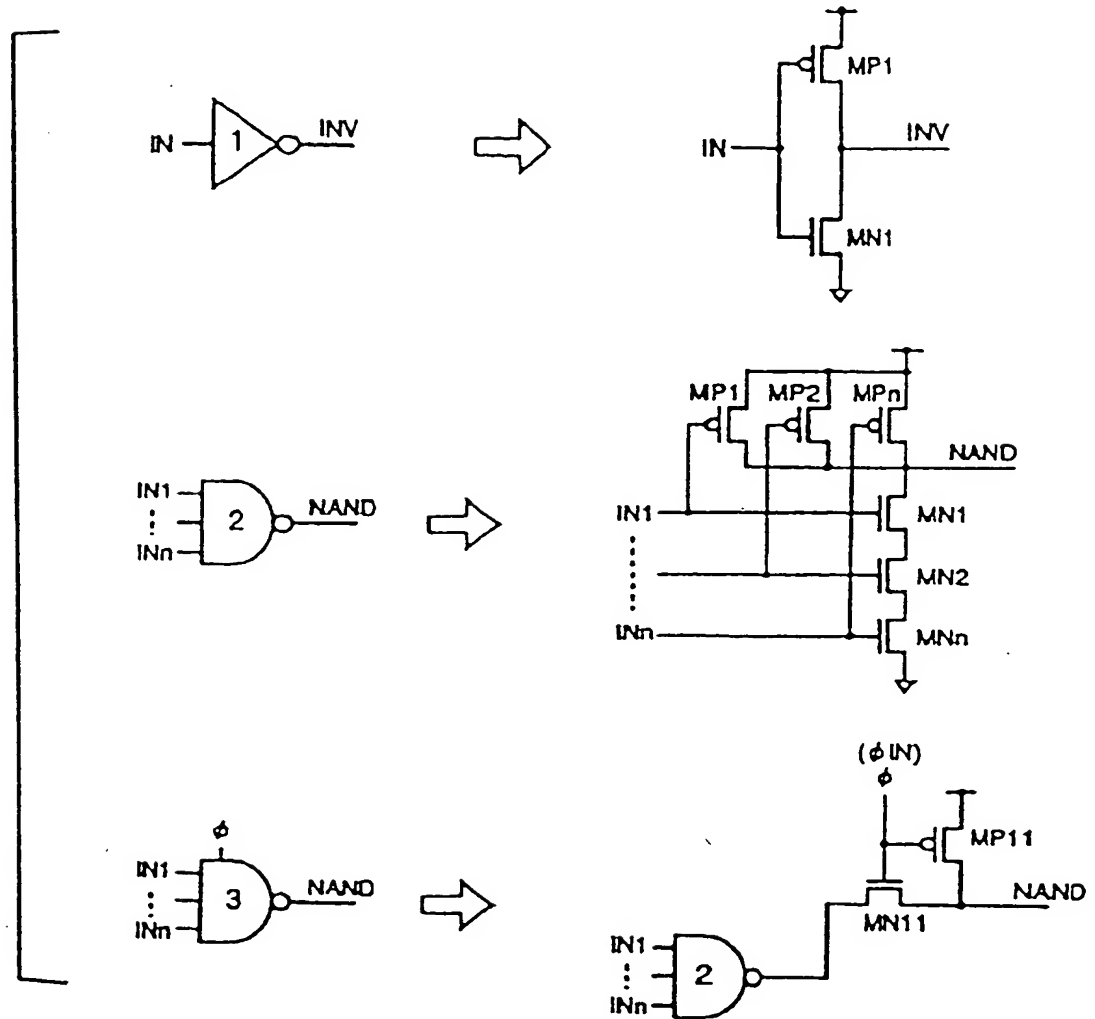


FIG. 18

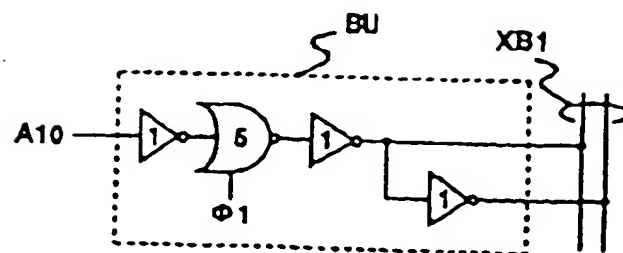


FIG. 19

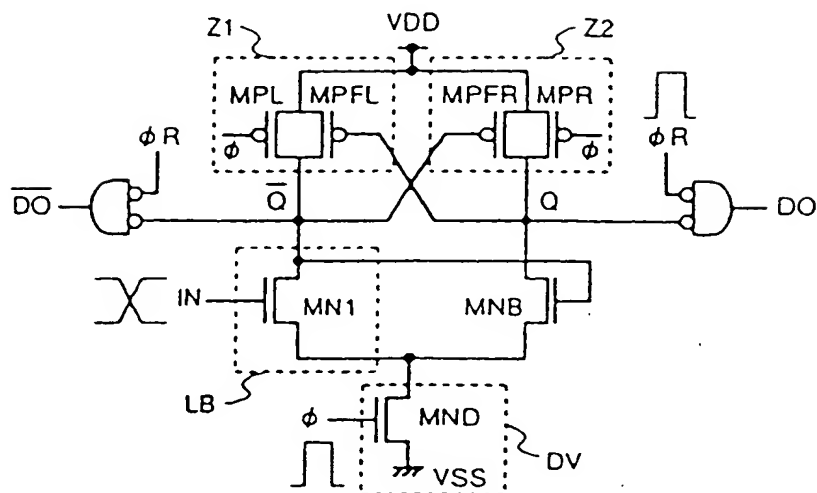


FIG. 20 PRIOR ART

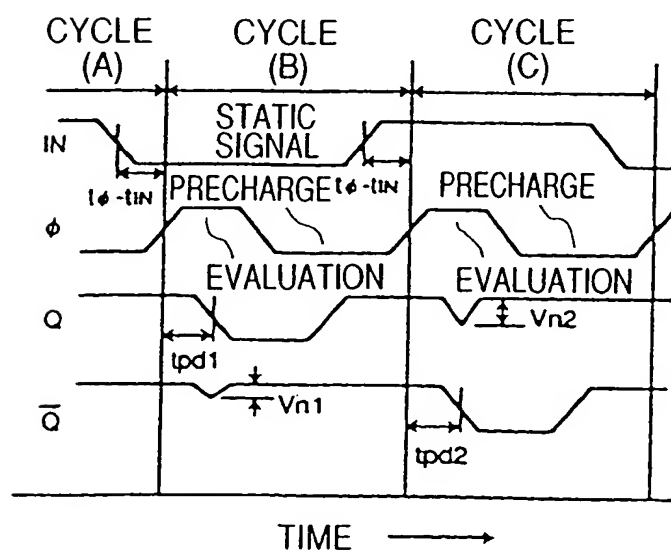
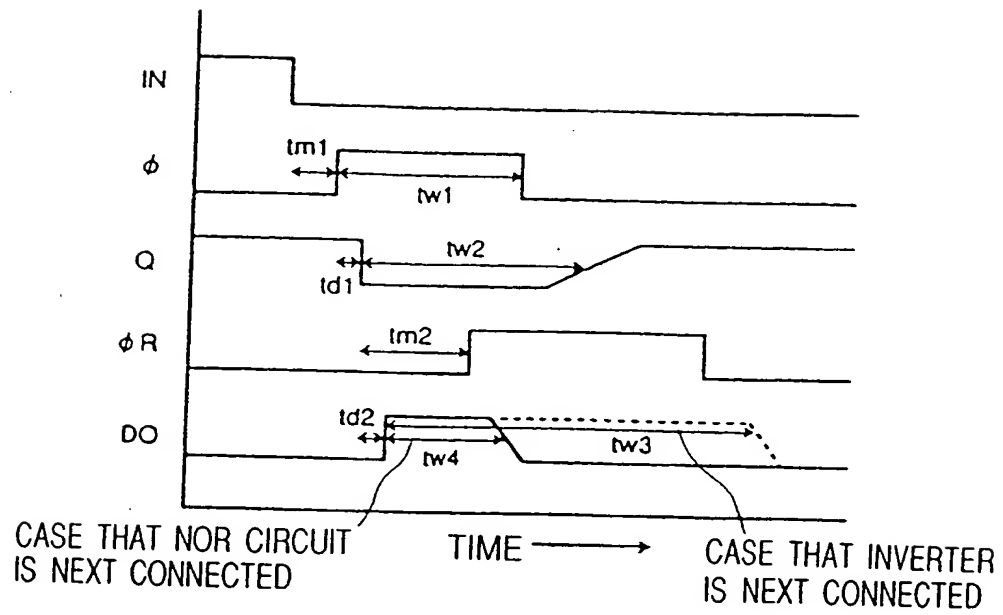


FIG. 21



[illegible]

The diagram shows the timing of a 4-bit ripple-carry adder. The signals and their transitions are as follows:

- IN:** A high-to-low transition at the start of the first clock cycle.
- ϕ :** A clock signal with a high pulse. The duration of the high pulse is $tw1$. The time from the rising edge of ϕ to the start of the Q transition is $tm1$.
- Q (T):** The output of the first stage. It has a delay $td1$ from the rising edge of ϕ before it begins to transition. The total time for the signal to settle to its new value is $tw2$.
- $\phi R2$:** A clock signal for the second stage. It has a delay $tm2$ from the rising edge of ϕ before it begins its high pulse.
- DO:** The output of the second stage. It has a delay $td2$ from the rising edge of $\phi R2$ before it begins to transition. The total time for the signal to settle to its new value is $tw3$.

The horizontal axis is labeled **TIME** with an arrow pointing to the right.

FIG. 24(a)

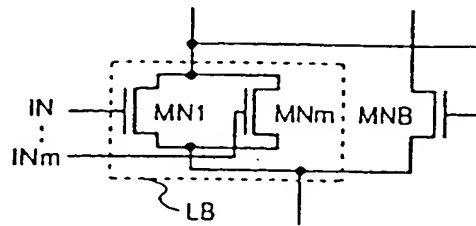


FIG. 24(b)

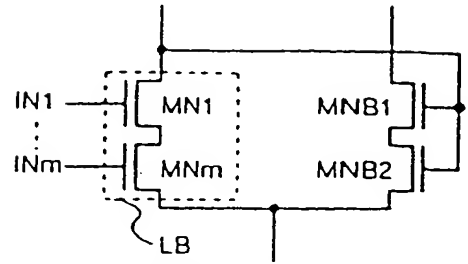


FIG. 24(c)

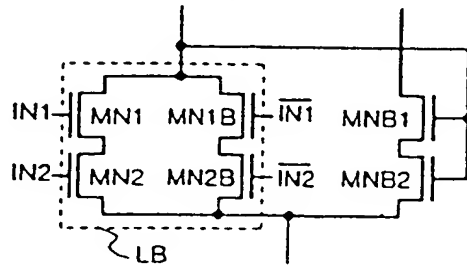


FIG. 24(d)

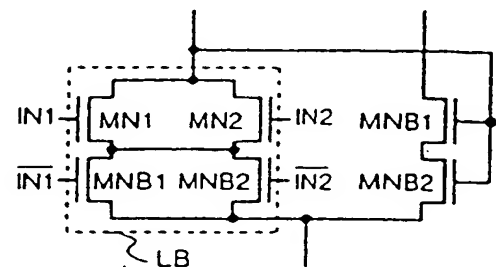


FIG. 24(e)

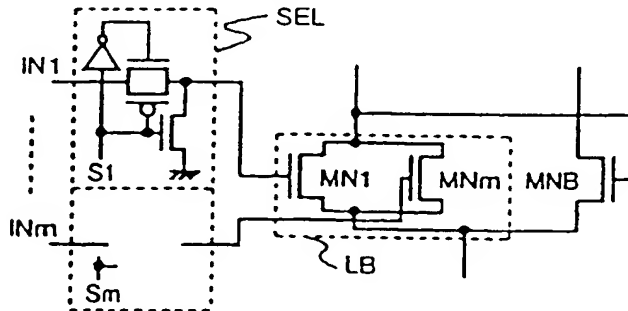


FIG. 24(f)

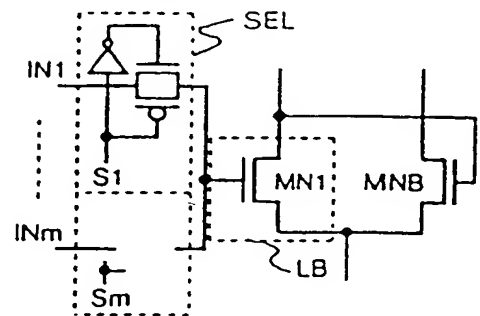


FIG. 24(g)

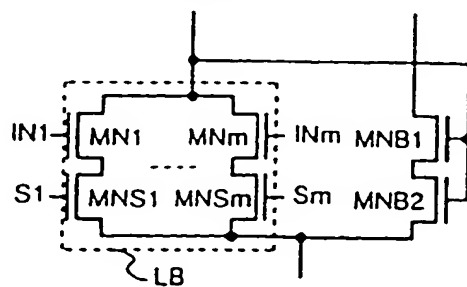


FIG. 25(a)

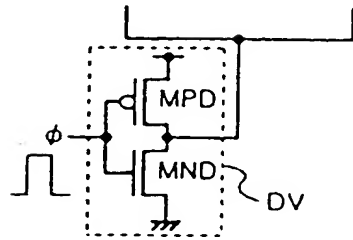


FIG. 25(b)

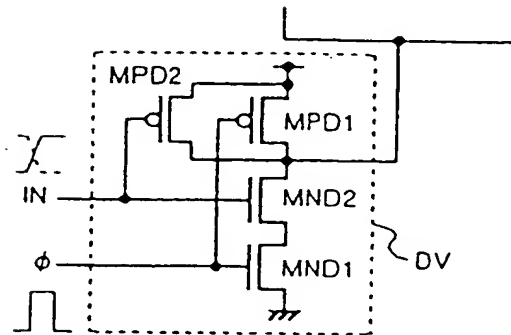


FIG. 26(a)

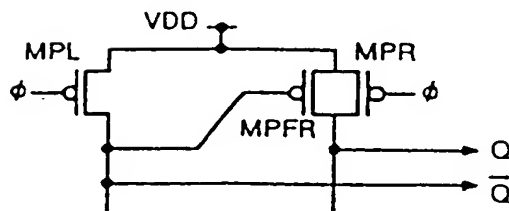


FIG. 26(b)

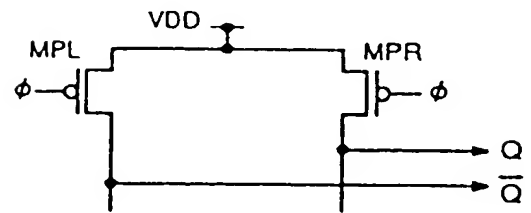


FIG. 26(c)

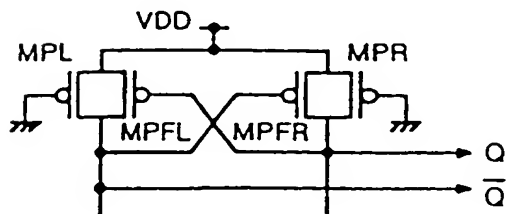


FIG. 27(a)

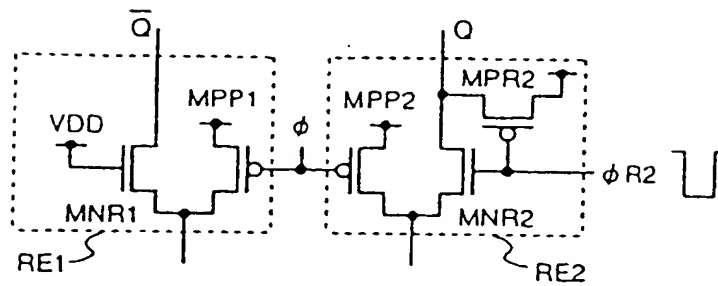


FIG. 27(b)

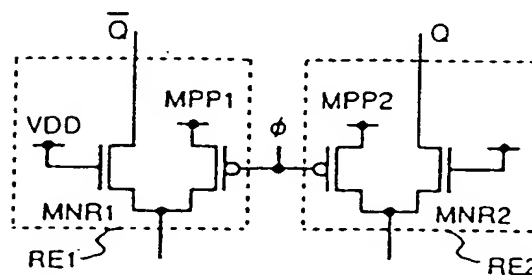


FIG. 28

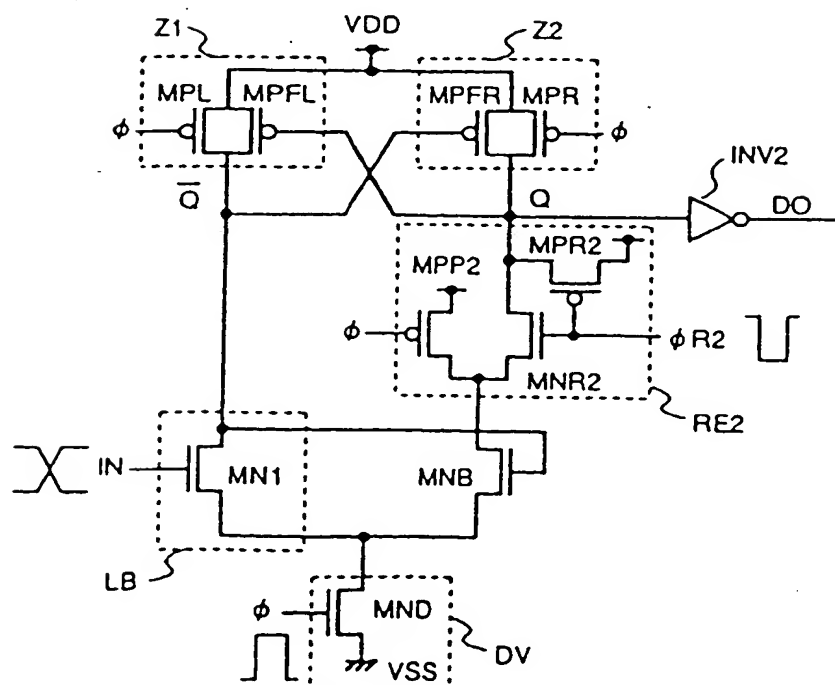


FIG. 29

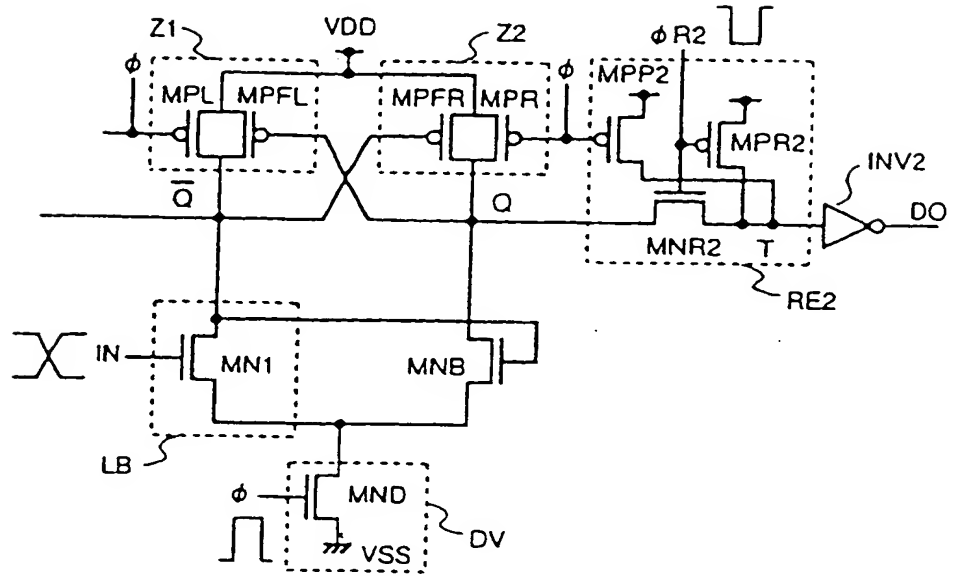


FIG. 30

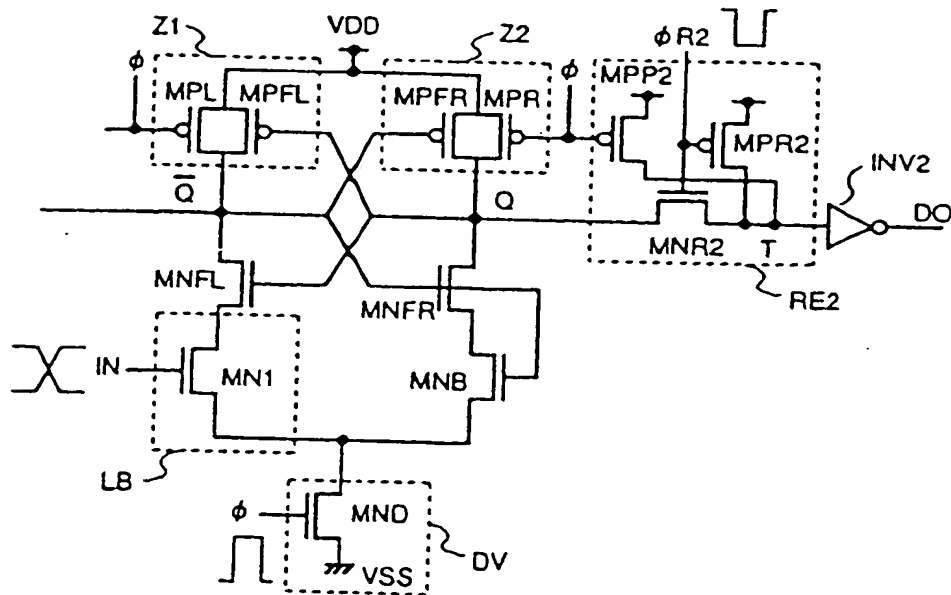


FIG. 31

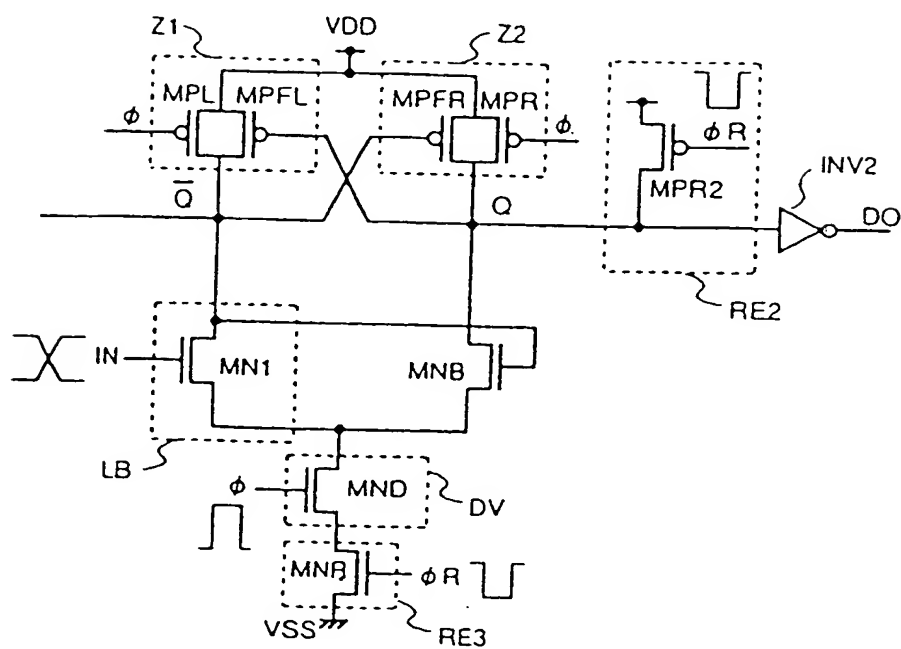


FIG. 32

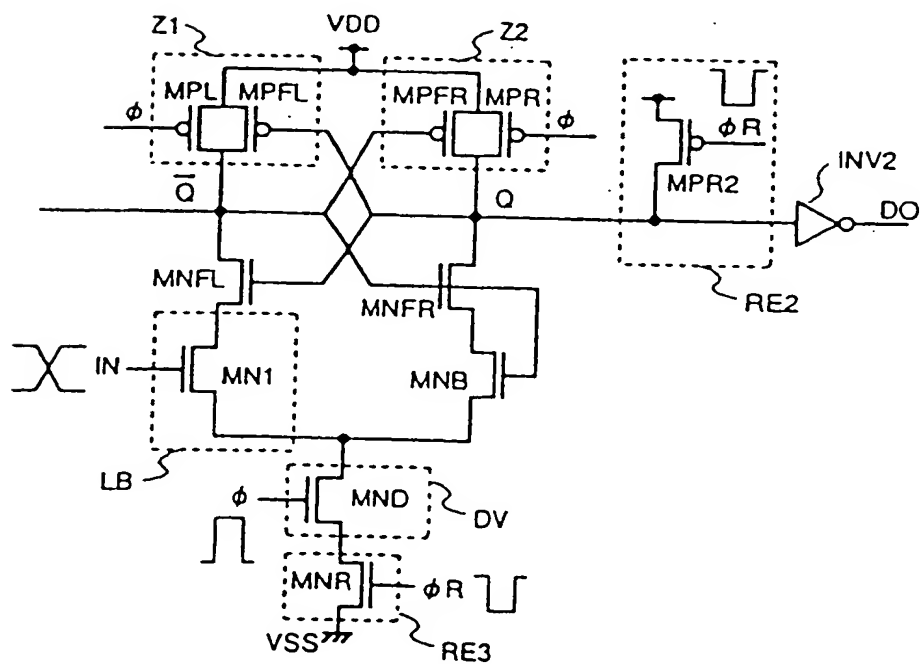


FIG. 33

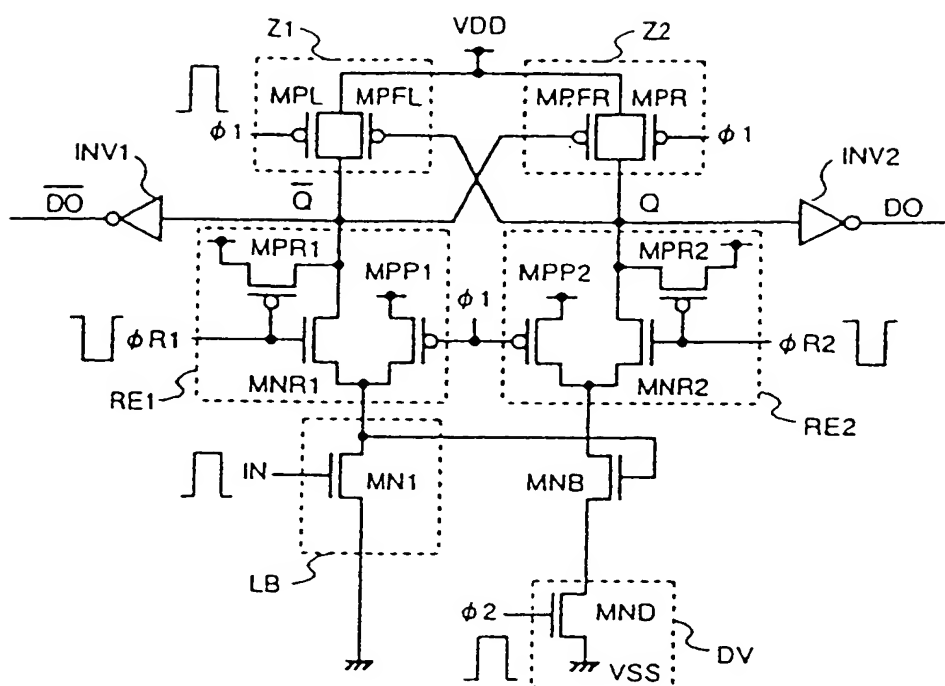


FIG. 34(a)

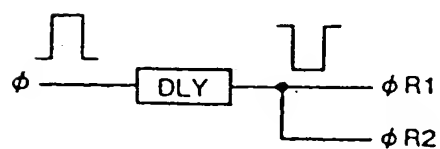


FIG. 34(b)

